MODELLING MEMORY AS CONDITIONAL PHENOMENA FOR A NEW THEORY OF COMPUTING

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Degree of Doctor of Philosophy

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Declaration

I declare that this is my own work and this thesis does not incorporate without acknowledgement any material previously submitted for a Degree or Diploma in any other University or institute of higher learning and to the best of my knowledge and belief, it does not contain any material previously published or written by another person except where the acknowledgement is made in the text.

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Signature of the supervisor: Date:

Dedicated To

My Loving

Mother, Father,

Husband, Son Vikum & Daughter Imandi

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Abstract

Computation in Von-Neumann architecture was quite different from the computation in the human mind, which processes in association with the brain by improving quality, accuracy and speed over the generations of execution of instructions. It was argued that this difference has been primarily caused by the separation of memory from processor, which results in delay in processing in the Von-Neumann architecture. Therefore, to improve computational efficiency on Von-Neumann architecture, various hardware and software level improvements have been introduced. In this sense, many researches were done in order to produce hardware level solutions, but there are limited researches to produce software level solutions. As such researches into develop new computing models at software level has been a research challenge. Our research has also discovered that despite the neuroscience of brain has inspired various computing models, behavior of mind has not been exploited to build models for computation.

As inspired by a theory of mind from an Eastern philosophy, Theravada Buddhism, we postulate the memory as a result of processing, and the memory and processing are not separated. The mind as a processor executes a conditional flow of thoughts pertaining to five-sense doors or the mind itself. The processing mechanism in the mind results an evolving memory. This thesis presents a novel **S**ix-State Processing Model (SSPM), which implements the processing in the mind and causing an evolving memory to improve processing speed of the computer. The six-state of SSPM encompasses New, Ready, Running, Blocked, Sleep, and Terminate, where the states Sleep and Terminate are new and are variations of the Exit in five-state model. Further, the SSPM has a set of newly defined transitions Ready-Ready, Sleep-Ready, Running-Ready, Running-Sleep, and Ready-Terminate that are associated with the concepts exploited from the Causal Relations of Buddhist Theory of Mind. Due to these states and transitions, the new model SSPM exhibits three distinct features, namely, internal and external processes, continuous processing, and a smaller tactics memory. Altogether, the SSPM works as a mind-like computer.

The evaluation of the SSPM has been conducted both in empirical level and the theoretical level. The empirical level testing was carried out separately for several computing programs that have been customized by the SSPM, where a Fraction Calculator (FC), a Quadratic Equation Solver (QES), a Sorting Program, and a Simulated Process Scheduler (PS) were among the programs. Further, the customized programs were named as SSPM-FC, SSPM-QES, SSPM-Sorting, and SSPM-PS. In fact, SSPM-FC considered a set of operations that included Plus, Minus, Multiplication, and Division, while the SSPM-Sorting had two categories such as SSPM-S-Insertion and SSPM-S-Equal. Furthermore, SSPM-FC (with Plus, Minus, and Multiplication), SSPM-QES, SSPM-Sorting (SSPM-S-Insertion, and SSPM-S-Equal), and SSPM-PS were tested separately under several testing scenarios to check their ability to gain improvements in the subsequent program execution cycles. Hence, it could prove the ability of the SSPM-system to improve the computing efficiency of the system in consecutive execution cycles

of the system. Next, with SSPM-FC, SSPM-QES, and SSPM-Sorting, it could be demonstrated that how the smaller tactics memory is improved over the time. In addition to that, the speedups gained by the SSPM-S-Insertion and the SSPM-S-Equal with compared to the original Quicksort were compared with the speedups gained by the quicksort programs implemented with some other computing approaches. There, the SSPM-S-Equal case showed speedup with compared to the original quicksort for all the tested lists (number of elements were varying from approximately 2 to 4M). However, the SSPM-S-Insertion had limiting conditions in showing the better performance. So then, the smaller tactics memory with the SSPM-Sorting could be organized and the appropriate mechanism could be selected as per the requirements over program execution cycles improving the computing power of the system. Finally, to evaluate the model in the theoretical level, SSPM has been simulated with a Turing Machine. Afterwards, checking the satisfiability, it has been proved the NP-completeness of SSPM. Hence, its computability and the real-world applicability has been theoretically proved. Overall, it has been able to prove that the solutions can be provided faster over subsequent execution cycles by modelling memory as conditional phenomena and leads to a new theory of computing.

Keywords: Evolving Tactics Memory, Six-State Processing Model, Continuous Processing, NP Complete, Special Compiler, 24-Causal Relations

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List of Abbreviations

ADAPTON	- Compassable, Demand Driven Incremental Computing
BT	- Buddhist Theory
BTM	- Buddhist Theory of Mind
CDDG	- Concurrent Dynamic Dependency Graph
CAS	- Column Address Signal
CL	- CAS Latency
CBRAM	- Conductive Bridge Random Access Memory
CPU	- Central Processing Unit
CR	- Causal Relation
CUDA	- Compute Unified Device Architecture
DDG	- Dynamic Dependency Graph
DRAM	- Dynamic Random Access Memory
EC	- Evolutionary Computing
EPROM	- Erasable Programmable Read Only Memory
FC	- Fraction Calculator
FCFS	- First Come First Serve
GA	- Genetic Algorithm
GPGPU	- General-Purpose computing on Graphics Processing Unit
GPU	- Graphics Processing Units
I/O	- Input/ Output
IC	- Incremental Computing
IDE	- Integrated Development Environment
IPC	- Inter Process Communications
ITS	- Throughput Target Scheme
LSTM	- Long Short Term Memory
LTM	- Long Term Memory
MAS	- Multi Agent Systems
MPI	- Misses Per Instruction

NMR	- Nuclear Magnetic Resonance
NTM	- Non deterministic Turing Machine
OS	- Operating System
PCM	- Phase Change Memory
PS	- Process Scheduler
QES	- Quadratic Equation Solver
RAM	- Random Access Memory
ROM	- Read Only Memory
RRAM	- Resistive Random Access Memory
SAC	- Self-Adjusting Computing
SAIL	- Self-Adjusting Imperative Language
SQUID	- Superconducting Quantum Interference Device
SSPM	- Six-State Continuous Processing Model
STM	- Short Term Memory
STT-MRAM	- Spin-Transfer-Torque-Magnetic Random Access Memory
TM	- Turing Machine
VNA	- Von Neumann Architecture
WEIS	- Instruction weighted speedup Targeted Scheme