

**FPGA IMPLEMENTATION OF EEG CLASSIFIER
USING LDA**

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degree Master of Science in Electronics and Automaton Engineering

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Declaration by candidate

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ABSTRACT

FPGA implementation of EEG classifier using LDA

Supervised by: Dr. S. Thayaparan

Key words: *LDA, EEG, FPGA, DWT, HDL*

Design and implementation of feature classification in Electroencephalography (EEG) signal processing system on Field Programmable Gate Array (FPGA) hardware platform is presented in this thesis. Today there is a growing demand for medical devices which process EEG signals, for which, it is important to implement the EEG processing system in hardware instead of software. Processing of EEG signals consist of extracting features from EEG signal and then processing those features to classify the signals. As of today, in most of EEG processing systems, classification part is done on software platform even though the feature extraction is done on hardware. In this project, classification is done with Linear Discriminant Analysis (LDA), based on the features extracted using Discrete Wavelet Transform (DWT), for EEG signals obtained through PhysioNet website. The hardware implementation was done on Field Programmable Gate Array (FPGA) platform using SystemVerilog Hardware Description Language (HDL). Final design has minimum resource utilization, hence is able implement on Basys 3 Artix-7 FPGA Trainer Board with the accuracy of 80%. Therefore, it is concluded this design is suitable for developing low cost, marketable products like sleep detectors for automobile drivers. Nevertheless, ultimate goal is to design a simple Application Specific Integrated Circuit (ASIC) chip, which can extract features and classify EEG, so that the full system can be implemented on a portable mobile device without using software platform.

To beloved Parents and Teachers

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TABLE OF CONTENTS

ABSTRACT	iv
ACKNOWLEDGEMENT	vi
TABLE OF CONTENTS	vii
LIST OF FIGURES	x
LIST OF TABLES	xii
LIST OF ABBREVIATIONS	xiii
Chapter 1	1
INTRODUCTION	1
1.1 Problem Identification	1
1.2 Motivating for the research	2
1.3 Existing solutions and technologies	2
1.4 Novel Contribution	3
Chapter 2	4
HARDWARE IMPLEMENTATION	4
2.1 EEG feature extraction	4
2.1.1 Obtaining EEG signals.....	4
2.1.2 What features to extract?.....	7
2.1.3 Discrete Wavelet Transform	7
2.1.4 Approximations and Details calculation	9
2.2 Classification of EEG signals	9
2.2.1 Selection of classification method	10
2.2.2 Classification using Linear Discriminant Analysis.....	11
2.3 Architecture design	14
2.3.1 Algorithm for the full system.....	14
2.3.2 Architecture of the full design	15
2.2.3 Requirements to process EEG signals offline	16

2.4 MATLAB implementation	16
2.4.1 Classification system.....	16
2.4.2 Wavelet and fixed points widths selection.....	18
2.5 RTL Implementation	20
2.5.1 Architecture of RTL design	20
2.5.2 Finite State Machine in the Arbiter.....	21
2.5.3 Fixed point calculations on Verilog.....	22
2.5.4 Simulations	25
2.6 FPGA Implementation	25
2.6.1 FPGA design flow.....	25
2.6.2 Selection of a FPGA development board.....	26
2.6.3 Specifying Constraints using XDC	28
2.6.4 Timing Closure	30
2.6.5 Power Utilization	31
2.7 Feasibility on Arduino implementation	31
2.7.1 Implementation on Arduino Mega 2650.....	31
2.7.2 Necessities to implement on FPGA	33
Chapter 3	34
RESULTS AND DEMONSTRATION	34
3.1 Timing and Power results for FPGA implementation	34
3.1.1 Modular timing analysis.....	36
3.2 Simulation results	37
3.2 Demonstration on FPGA development board	40
3.4 Accuracy of hardware implemented design	40
3.5 Comparison of hardware and software results	42
Chapter 4	43
DISCUSSION	43

4.1 Commonly Used Tools	43
4.1.1 Vivado Design Suite	43
4.1.2 Xilinx ISE	44
4.1.3 MATLAB.....	44
4.1.4 Arduino IDE.....	45
4.2 Problems and solutions	45
4.3 Recourse utilization in FPGA	46
4.3.1 Issues due to resource utilization	47
Chapter 5	48
CONCLUSION AND FUTURE WORK	48
5.1 Conclusion	48
5.2 Future work	48
BIBLIOGRAPHICAL REFERENCES	50