FPGA IMPLEMENTATION OF EEG CLASSIFIER USING LDA

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Degree of Master of Science

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Thesis submitted in partial fulfillment of the requirements for the degree Master of Science in Electronics and Automaton Engineering

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Declaration by candidate

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ABSTRACT

FPGA implementation of EEG classifier using LDA

Supervised by: Dr. S. Thayaparan

Key words: *LDA, EEG, FPGA, DWT, HDL*

Design and implementation of feature classification in Electroencephalography (EEG) signal processing system on Field Programmable Gate Array (FPGA) hardware platform is presented in this thesis. Today there is a growing demand for medical devices which process EEG signals, for which, it is important to implement the EEG processing system in hardware instead of software. Processing of EEG signals consist of extracting features from EEG signal and then processing those features to classify the signals. As of today, in most of EEG processing systems, classification part is done on software platform even though the feature extraction is done on hardware. In this project, classification is done with Linear Discriminant Analysis (LDA), based on the features extracted using Discrete Wavelet Transform (DWT), for EEG signals obtained through PhysioNet website. The hardware implementation was done on Field Programmable Gate Array (FPGA) platform using SystemVerilog Hardware Description Language (HDL). Final design has minimum resource utilization, hence is able implement on Basys 3 Artix-7 FPGA Trainer Board with the accuracy of 80%. Therefore, it is concluded this design is suitable for developing low cost, marketable products like sleep detectors for automobile divers. Nevertheless, ultimate goal is to design a simple Application Specific Integrated Circuit (ASIC) chip, which can extract features and classify EEG, so that the full system can be implemented on a portable mobile device without using software platform.

To beloved Parents and Teachers

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